Main Memory in HPC: Do We Need More, or Could We Live with Less?

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MEMORY IN CURRENT HPC SYSTEMS
* Current HPC systems are dominated by x86 architectures coupled with 2-3GB of main memory per core
* 3D memory provides better performance and energy efficiency but lower capacities compared to conventional DIMMs
* Important to analyze memory requirements of HPC benchmarks and production HPC applications for the adoption of 3D memories

HIGH-PERFORMANCE LINPACK (HPL)
* HPL is CPU bound, and almost reaches theoretical peak FLOP/s
* HPL performance depends on memory capacity per core:
  - Performance first increases, then reaches saturation point
  - Saturation point is proportional to the number of processes
  - Saturation point moves towards larger capacities when increasing the number of processes

CONCLUSION
* For HPC system with tens or hundreds of cores, reaching HPL saturation point requires approx. 2GB of memory per core

HIGH-PERFORMANCE CONJUGATE GRADIENTS (HPCG)
* HPCG performance depends on available memory bandwidth
* HPCG performance depends on memory capacity per core:
  - Performance first increases, then reaches saturation point
  - Saturation point is proportional to the number of processes
  - Saturation point remains constant, roughly 512MB per process

CONCLUSION
* Reaching HPCG saturation point requires roughly 512MB per process and does not increase with the number of processes

PRODUCTION HPC APPLICATIONS

EXPERIMENTAL SETUP
* Unified European Application Benchmarks Suite on MareNostrum:
  ALYA, BQCD, CP2K, GADGET, GENE, GROMACS, NAMD, NEMO, QE, SPECFEM3D

ANALYSIS
* Per-process memory footprints change with the number of processes
* Select representative number of processes:
  1. HPC category:
     - Capacity computing [job throughput]
     - Capability computing [execution time]
     - Application scalability
  2. Metrics of interest:
     1. Execution time
     2. Cost [CPU hours]
     3. Energy consumption

CONCLUSION
* We detect bimodal distribution of memory requirements:
  1. Most applications have per-core footprints of hundreds of MB, use cases that could be a success story for 3D memory chiplets
  2. We detect applications that require gigabytes of memory per-core that could be provided with hybrid (3D + DIMMs) memories

FURTHER READING

Darko Zivanovic, Milan Radulovic, Germain Lloret, David Zaragoza, Janko Straznuk, Paul M Carpenter, Petar Radojkovic, Eduard Ayguadé.
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